DECLARATION AND POWER OF ATTORNEY

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled: A SEMICONDUCTOR INTEGRATED CIRCUIT HAVING COMPRESSION CIRCUITRY FOR COMPRESSING TEST DATA, AND THE TEST SYSTEM AND METHOD UTILIZING THE SEMICONDUCTOR INTEGRATED CIRCUIT; the specification of which is attached hereto.

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims.

I acknowledge the duty to disclose information which is material to patentability as defined in Title 37 of the Code of Federal Regulations, Section 1.56.

I hereby claim the benefit under Title 35 of the United States Code, Section 120 to which I am entitled and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35 of the United States Code, Section 112, I acknowledge the duty to disclose information which is material to patentability as defined in Title 37 of the Code of Federal Regulations, Section 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application.

Inventor's Full Name:	Roland	Ochoa		
	(First) (M	II) (Last)		
Inventor's Signature:	Raling Ochoa	Date: 12-9-94		
Citizenship:	United States			
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City, State and Country of Residence	Boise, Idaho United States of America			
Inventor's Full Name:	Gregory I (First) (M	L. Cowan II) (Last)		
Inventor's Signature:	July & Com	Date: 9-0EC-94		
Citizenship:	United States	i y		
Post Office Address:	1554 Riverstone Lane	e, #304		
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Inventor's Full Name:	Roland		Ochoa	
	(First)	(MI)	(Last)	
Inventor's Signature:	Ralind Och	12.	Date: 12-9-9	ý
Citizenship:	United States	7		
Post Office Address:	4185 Kilarney			
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City, State and Country of Residence	Boise, Idaho Ui	nited States o	of America	
Inventor's Full Name:	Gregory (First)	L. (MI)	Cowan · (Last)	
Inventor's Full Name: Inventor's Signature:	Trung & Ca	<u></u>	Date: 9-0EC-	-94
Citizenship:	United States	s •		
© Post Office Address:	1554 Riverstone	e Lane, #304		
City, State and	Boise, Idaho 83	3706	•	
Country of Residence	Boise, Idaho U	nited State o	f America	

inventor's rull Name:		<u>IVI.</u>	Fierce	
	(First)	(MI)	(Last)	
Inventor's Signature:	-Bin	N. Pine	7_Date: /2 - ·	<u>9 - 94</u>
Citizenship:	Untied State	es	-	
Post Office Address:	1064 East C	ayman Drive		
City State and	Meridian, Id	laho 83642		
City, State and Country of Residence	Meridian, Io	laho United Stat	es of America	······································

SUPPLEMENTAL 'LARATION FOR PATENT APPLICATION (WITH PC R OF ATTORNEY)

As an inventor named below or on any attached continuation page, I hereby declare that: My residence, post office address and citizenship are as stated next to my name. I believe that I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled A SEMICONDUCTOR INTEGRATED CIRCUIT HAVING COMPRESSION CIRCUITRY FOR COMPRESSING TEST DATA, AND THE TEST SYSTEM AND METHOD FOR UTILIZING THE SEMICONDUCTOR INTEGRATED CIRCUIT, the specification of which (check one): ☐ is attached hereto. as PCT international application no. _____ and was amended under PCT Article 19 on ____ I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above. I acknowledge the duty to disclose to the U.S. Patent and Trademark Office all information known to me to be material to the patentability of the subject matter claimed in this application, as "materiality" is defined in Title 37, Code of Federal Regulations § 1.56. I hereby claim foreign priority benefits under Title 35, United States Code, § 119(a)-(d) or § 365(b) of any foreign application(s) for patent or inventor's certificate or § 365(a) of any PCT international application(s) designating at least one country other than the United States of America listed below and on any attached continuation page and have also identified below and on any attached continuation page any foreign application for patent or inventor's certificate or any PCT international application(s) designating at least one country other than the United States of America having a filing date before that of the application(s) on which priority is claimed. Prior foreign/PCT application(s): Priority Claimed (country) (number) (day/month/year filed) (number) (country) (day/month/year filed) No I hereby claim the benefit under Title 35, United States Code, § 120 of any United States application(s) or § 365(c) of PCT international application(s) designating the United States of America listed below and on any attached continuation page and, insofar as the subject matter of each of the claims of this application is not disclosed in any such prior application in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the aduty to disclose to the U.S. Patent and Trademark Office all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations § 1.56 which became available between the filing date of such prior application and the national or PCT international filing date of this application: 08/881,946 June 25, 1997 (filing date) Patented - 5,864,565 (application serial no.) (status - pending, patented or abandoned) 08/353,404 December 9, 1994 Abandoned (status - pending, patented or abandoned) (application serial no.) (filing date) 08/077,182 June 15, 1993 Abandoned (application serial no.) (filing date) (staus) - pending, patented or abandoned) I hereby claim the benefit under Title 35, United States Code, § 119(e) of any United States provisional application(s) listed below: (provisional application no.) (filing date) I hereby appoint the following Registered Practitioners to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith: David V. Trask, Reg. No. 22,012 William S. Britt, Reg. No. 20,969 Laurence B. Bond, Reg. No. 30,549 Joseph A. Walkowski, Reg. No. 28,765 James R. Duzan, Reg. No. 28,393 Allen C. Turner, Reg. No. 33,041 Edgar R. Cataxinos, Reg. No. 39,931 Stephen R. Christian, Reg. No. 32,687 Kent S. Burningham, Reg. No. 30,453 Brick G. Power, Reg. No. 38,581 Kenneth B. Ludwig, Reg. No. 42,814 Paul C. Oestreich, Reg. No. 44,983 Devin R. Jensen, Reg. No. 44,805 Eleanor V. Goodall, Reg. No. 35,162 Samuel E. Webb, Reg. No. 44,394 Kerry D. Tweet, Reg. No. 45,959 David L. Stott, Reg. No. 43,937 Bradley B. Jensen, Reg. No. 46,801 Michael L. Lynch, Reg. No. 30,871 Charles B. Brantley II, Reg. No. 38,086 Address all correspondence to: Joseph A. Walkowski, telephone no. (801) 532-1922. TRASK BRITT P.O. BOX 2550 Salt Lake City, Utah 84110

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued

Date 2-22-0

Full name of first joint inventor: Roland Ochoa

Inventor's signature Residence: Boise, Idaho Citizenship: USA

. Andir

Post Office Address: 4185 Kilarney, Boise, ID 83704-3334

DECLARATION FOR PATENT APPLICATION

(continuation page)

Invention title: A SEMICONDUCTOR INTEGRATED CIRCUIT HAVING COMPRESSION CIRCUITRY FOR COMPRESSING TEST DATA, AND THE TEST SYSTEM AND METHOD FOR UTILIZING THE SEMICONDUCTOR INTEGRATED CIRCUIT

Inventor name(s) appearing on first declaration page: Roland Ochoa

Additional original, first and joint inventor(s):

Full name of second joint inventor: Gregory L. Cowan July	Have Date 23-FEB-2001	
Residence: Boise, Idaho		
Citizenship: USA		
Post Office Address: 1554 Riverstone Lane, #304, Boise, ID 83706		
Full name of third joint inventor: Kim M. Pierce		
Inventor's signature	Date	
Residence: Meridian, Idaho		
Olston and the FIGA		

Citizenship: USA Post Office Address: 1064 East Cayman Drive, Meridian, ID 83642

SUPPLEMENTAL 1 LARATION FOR PATENT APPLICATION (WITH Pt ... R OF ATTORNEY)

As an inventor named below or on any attached continuation page, I hereby declare that:

My residence, post office address and citizenship are as stated next to my name.

Residence: Boise, Idaho Citizenship: USA

Post Office Address: 4185 Kilarney, Boise, ID 83704-3334

I believe that I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled A SEMICONDUCTOR INTEGRATED CIRCUIT HAVING COMPRESSION CIRCUITRY FOR COMPRESSING TEST DATA, AND THE TEST SYSTEM AND METHOD FOR UTILIZING THE SEMICONDUCTOR INTEGRATED CIRCUIT, the specification of which (check one):

		ted States application serial no. 09/175,518. rnational application no and was amend	ded under PCT Article 19 on		
-	I hereby state that I have reviewed and unreferred to above.	nderstand the contents of the above-identified specific	cation, including the claims, as amended	l by any amendment	
1		U.S. Patent and Trademark Office all information k iality" is defined in Title 37, Code of Federal Regula		ability of the subject	
]	certificate or § 365(a) of any PCT internation attached continuation page and have also ider PCT international application(s) designating a which priority is claimed.	nder Title 35, United States Code, § 119(a)-(d) or § nal application(s) designating at least one country oth ntified below and on any attached continuation page at least one country other than the United States of A	ter than the United States of America list any foreign application for patent or inv	ted below and on any entor's certificate or a	
]	Prior foreign/PCT application(s):			Priority Claimed	
-	(number)	(country)	(day/month/year filed)	Yes No	
	(number)	(country)	(day/month/year filed)	Yes No	
÷c	ury to disclose to the U.S. Patent and Trade	application in the manner provided by the first paragrams. Office all information known to me to be mate etween the filing date of such prior application and to June 25, 1997 (filing date)	rial to patentability as defined in Title 3 he national or PCT international filing of Patented - 5,8	7, Code of Federal late of this application:	
	•	· -	(status - pending, patented or abando		
¥	08/353,404 (application serial no.)	December 9, 1994 (filing date)	Abando (status - pending, patent	oned ed or abandoned)	
	08/077,182 (application serial no.)	<u>June 15, 1993</u> (filing date)	Aband (staus) - pending, pat		
THE STATE OF	I hereby claim the benefit under Title 35,	United States Code, § 119(e) of any United States p	rovisional application(s) listed below:		
juš -	(provisional application no.)	(filing date)			
t	I hereby appoint the following Registered Inerewith: David V. Trask, Reg. No. 22,012 Joseph A. Walkowski, Reg. No. 28,765 Edgar R. Cataxinos, Reg. No. 39,931 Brick G. Power, Reg. No. 38,581 Devin R. Jensen, Reg. No. 43,937 Michael L. Lynch, Reg. No. 43,937	Practitioners to prosecute this application and to trar William S. Britt, Reg. No. 20,969 James R. Duzan, Reg. No. 28,393 Kent S. Burningham, Reg. No. 30,453 Kenneth B. Ludwig, Reg. No. 42,814 Eleanor V. Goodall, Reg. No. 35,162 Kerry D. Tweet, Reg. No. 45,959 Charles B. Brantley II, Reg. No. 38,086	Laurence B. Bond, Reg. No. 30,54 Allen C. Turner, Reg. No. 33,041 Stephen R. Christian, Reg. No. 32 Paul C. Oestreich, Reg. No. 44,98 Samuel E. Webb, Reg. No. 44,394 Bradley B. Jensen, Reg. No. 46,80	687 3	
A	ddress all correspondence to: Jose TR P.O	eph A. Walkowski, telephone no. (801) 532-1922. ASK BRITT D. BOX 2550 t Lake City, Utah 84110			
b	nd further that these statements were made w	erein of my own knowledge are true and that all sta rith the knowledge that willful false statements and t nited States Code and that such willful false statemen	he like so made are punishable by fine o	or imprisonment, or	
	ull name of first joint inventor: Roland Ocho	Da Da	ate.		
13	ventor's signature	<i>D</i> a	in		

DECLARATION FOR PATENT APPLICATION

(continuation page)

Invention title: A SEMICONDUCTOR INTEGRATED CIRCUIT HAVING COMPRESSION CIRCUITRY FOR COMPRESSING TEST DATA, AND THE TEST SYSTEM AND METHOD FOR UTILIZING THE SEMICONDUCTOR INTEGRATED CIRCUIT

Inventor name(s) appearing on first declaration page: Roland Ochoa

Additional original, first and joint inventor(s):

Full name of second joint inventor: Gregory L. Cowan			
Inventor's signature	Date	-	
Residence: Boise, Idaho			
Citizenship: USA			
Post Office Address: 1554 Riverstone Lane, #304, Boise, ID 83706			
Full name of third joint inventor: Kim M. Pierce	Date	March	6.2002
Residence: Meridian, Idaho			- John State of the state of th

Citizenship: USA
Post Office Address: 1064 East Cayman Drive, Meridian, ID 83642